Code : 051402

B.Tech 4th Semester Examination, 2017

Computer Architecture

Time : 3 hours

Full Marks : 70

Instructions :

(i) There are **Nine Questions** in this Paper.

(ii) Attempt **Five** questions in all.

(iii) **Question No. 1 is Compulsory.**

(iv) The marks are indicated in the right-hand margin. Each question carry in equal marks.

1. Answer the following questions (any seven):

(a) Write the range of decimal integer can be represented by n-bit 2's complement representation.

(b) Justify the statement "Stack computer consists of an operation code only with no address field".

(c) What do you mean by Arithmetic shift left operation?

(d) What do you mean by locality of reference?

(e) What are the properties of an ideal instruction set computer.

(f) Define the term hardware polling.

(g) What do you mean by data hazards in pipelining?

(h) Explain indirect address mode, and how the effective address in calculated in this case.

(i) Explain the use of subroutine with the help of suitable example.

2. Why is read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs?

3. Explain the concept of virtual memory with the help of diagram. Explain how virtual address in mapped to actual physical address.

4. What is meant by Addressing Mode? Explain at least five different Addressing Modes with an example.

5. What are the different conflicts that will arise in pipeline (elaborate)? How do you remove the conflicts?

6. Explain Von Neumann Architecture. What are its drawbacks?

7. What is a page fault? What does a page fault signify? Explain the different page replacement algorithms which determine the page to be removed in case of full memory.

8. Why does I/O interrupt make more efficient use of the CPU? Explain the sequence of operations that take place in an interrupt driven I/O transfer.

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9. How many ROM chips are required to produce a memory capacity of 4096 bytes? How many address lines are required to access the 4096 bytes? How many of these addresses will be common to all these chips?

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